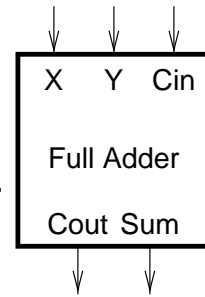




PART 2 (18 points) **Neatness and clarity will count!!**

(a. 9 points) Here is a block diagram for a full adder combinational circuit. Draw 3 copies of this diagram together with  $3 + 3 = 6$  input wires and 4 output wires. Label the input wires  $A_2, A_1, A_0$  and  $B_2, B_1, B_0$  and the output wires  $S_3, S_2, S_1, S_0$ . (The bits are named from high order,  $A_3$  for example, to low order or ones,  $A_0$  for example.) Draw the interconnections to make a combinational adder circuit for two 3 bit words. Be sure to explicitly indicate what signal is driving the carry-in input of the lowest order full adder circuit.



(b. 9 points) The logic portion of an ALU is to provide the four (bitwise) logic operations on words  $A$  and  $B$ :  $A + B$  (bitwise **OR**),  $A \cdot B$  (bitwise **AND**),  $A \oplus B$  (exclusive OR) and  $\bar{A}$  (bitwise **NOT**). Show the combinational circuit that will produce the  $i$ th data bit  $Y_i$  from  $A_i$  and  $B_i$  according to the value of two selector bits  $S_1 S_0$ . Your circuit should include a multiplexer and an exclusive or gate. Next to your circuit, write a table that shows what selector input value will select each logic operation.

PART 3 (23 points)

(a. 6 points) Apply the Karnaugh map method to find a minimal sum of products formula for the Boolean function plotted on this Karnaugh map. Show the blocks as well as the answer.

		B			
		00	01	11	10
A	0	0	1	1	0
	1	1	1	0	1
		C			

(b. 5 points) Fill in the truth table for the Boolean function that was plotted on the above Karnaugh

map:

A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

The Karnaugh map method specifies that the rectangular blocks (of size  $2^k$ ) used to cover the 1s should be as large as possible even if two blocks overlap.

(c. 4 points) What would be the disadvantage if somebody used a block whose size was not a power of 2, say, a block of 3 squares?

(d. 4 points) What would be the disadvantage if somebody used a block that was not as large as possible?

(e. 4 points) The following are two rows (out of 128) of a truth table. The other 126 rows are not shown because the **output value for each of them is 0**. Write the simplest boolean algebra formula for the function given by this truth table—It must be a single product of variables or

complements of variables.

A	B	C	D	E	F	G	Out
0	1	1	0	1	0	1	1
0	1	1	1	1	0	1	1

**ANSWER:**

PART 4 (13 points) Hexadecimal notation is used throughout this problem.  
Reference material on the instruction set architecture of Mano's basic computer:

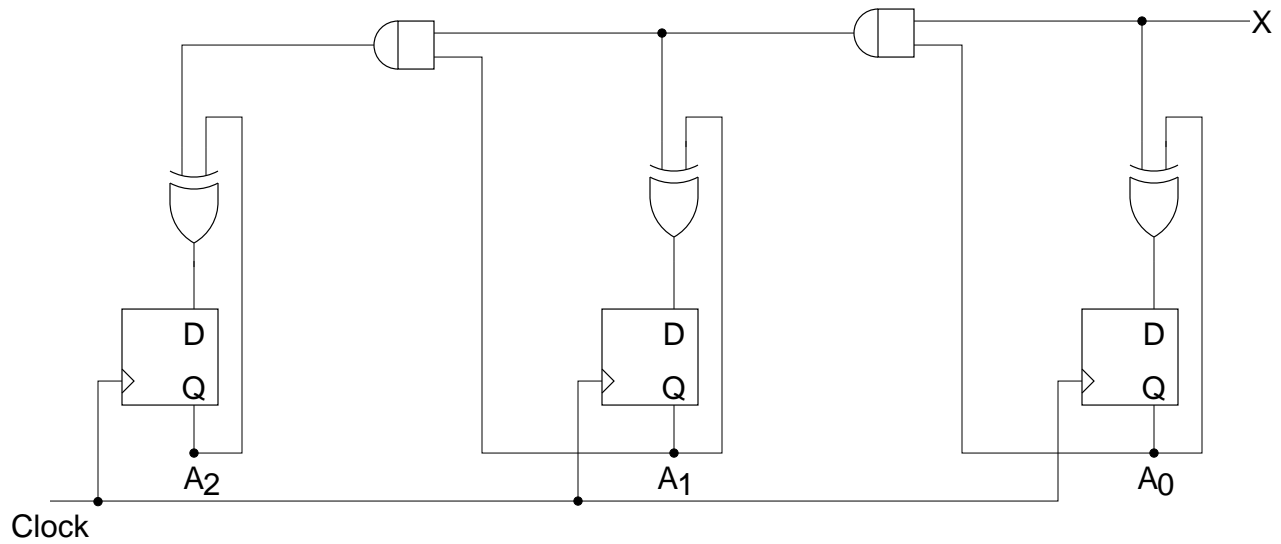
(a. 7 points) Write the instructions in the order that they are executed when the initial memory contents are given **below** and the computer is started with  $PC = 0$ . Note that some instructions should be written twice.

Address	Contents
0	2005
1	7010
2	6005
3	7001
4	4000
5	FFFF
6	A008
7	7001
8	0009
9	C009

(b. 3 points) Suppose the Mano basic computer is started, with the above memory contents as originally printed, with  $PC=6$ . What value is in the accumulator (AC) when it halts?\_\_\_\_\_

(c. 3 points) What does the Mano basic computer do if it is started with  $PC = 0$ ,  $AC = 0$ ,  $E = 0$  and the entire contents of memory equal to zero? Explain why.

PART 5 (10 points)



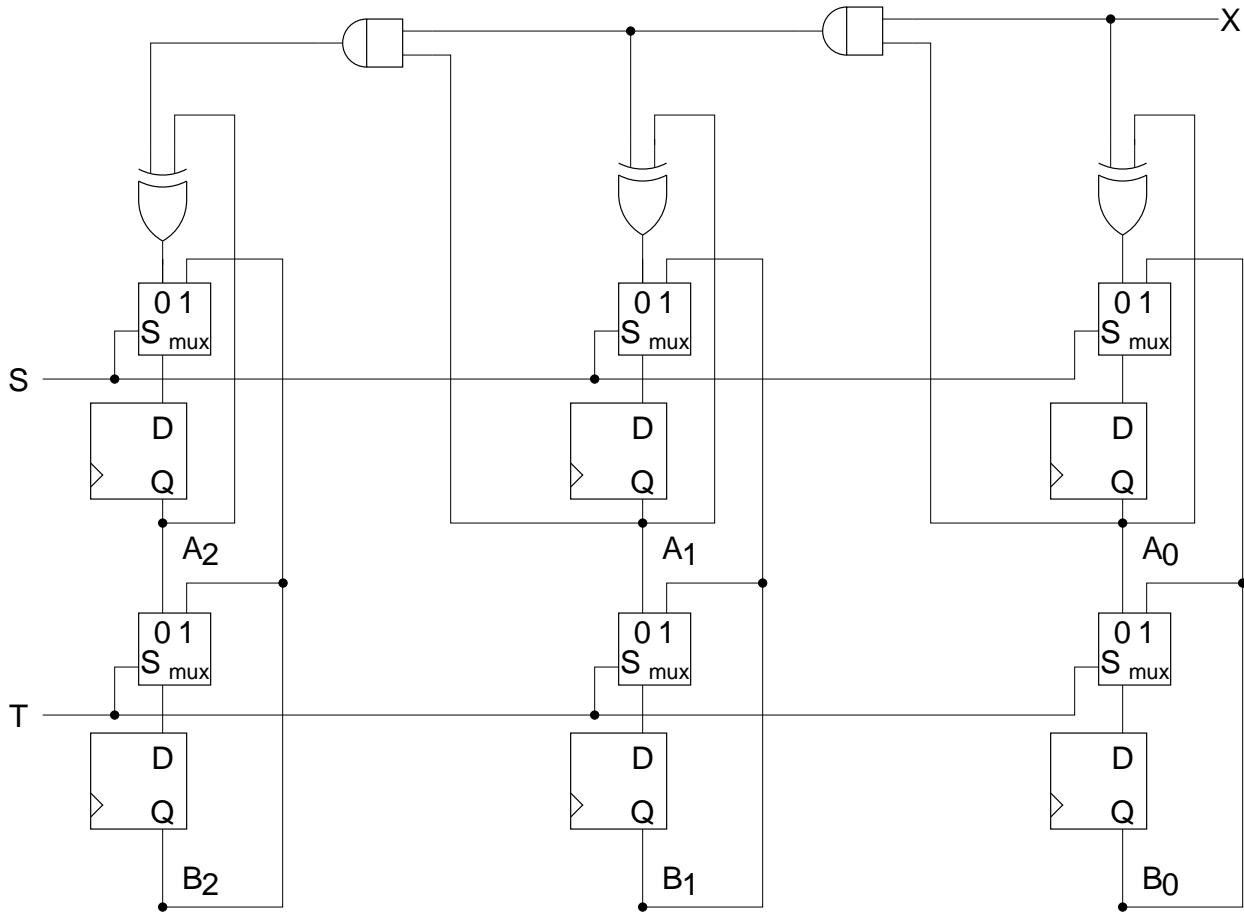
(a.) Fill in the state transition table and (b.) draw the state transition diagram for the above sequential circuit. **Neatness counts!** (You may use a single octal digit for the number  $(A_2A_1A_0)_{ten}$  if you wish.)

Table

$A_2$	$A_1$	$A_0$	$X$	$A_2$	$A_1$	$A_0$
0	0	0	0			
0	0	1	0			
0	1	0	0			
0	1	1	0			
1	0	0	0			
1	0	1	0			
1	1	0	0			
1	1	1	0			
0	0	0	1			
0	0	1	1			
0	1	0	1			
0	1	1	1			
1	0	0	1			
1	0	1	1			
1	1	0	1			
1	1	1	1			

Diagram

PART 6 (10 points)



Register Transfer Language is for describing hardware.

Write a description of this hardware in Register Transfer Language (Mano's notation): Use symbols  $A$  and  $B$  for the 3 bit registers  $A_2A_1A_0$  and  $B_2B_1B_0$  respectively.

The given sequential circuit has 6 D-type flip-flops. Three of them comprise one 3-bit register denoted by  $A$ . The other three flip-flops comprise another 3-bit register  $B$ . The circuit also has 3 single bit input wires  $X$ ,  $S$  and  $T$ . They function as "control inputs." The wire driving the 6 D flip-flop clock inputs is not shown for the sake of clarity. The combinational logic elements used are 2 **AND** gates, 3 exclusive-OR gates and 6 single bit 2-to-1 multiplexers.