

Announcement: The final exam will be given as scheduled on Tuesday, May 15, from 10:30 AM to 12:30 PM. It will be given with alternate seating in two rooms: LC-6(for even ids: 0,2,4,6,8) and LC-22(for odd ids: 1,3,5,7,9).

The final exam format will be similar to that of the midterms: closed book with 2 sheets of notes permitted (which could be double sided.) It will be comprehensive: 3/4 of the points will be on topics covered in the other 2 exams and 1/4 of the points will be on the later topics: System interconnection using buses, interrupts, pipelining, and memory hierarchies (with caches and virtual memories).

Reading: Patterson and Hennessy Chapter 7: Sections 7.1 through 7.4; concentrate on topics covered in the lectures.

Problem 1: Patterson and Hennessy problem 6.3: First, copy the code, write a NOP instruction under the `beq` and explain why that NOP instruction is necessary. Then, answer the question by modifying the code so the instruction in the delay slot (the NOP) is changed to one that does useful work. (You **will** have to make one or more additional modifications.) Finally, under the assumption that the loop runs 5 times (5 loads and adds) figure out (1) the number of clock steps used to execute all steps for the original code and (2) the number of clock steps used to execute your new, improved code. No stalls will occur because the ALU result is forwarded to the branch comparator in time for the branch decision to be made (see fig. 6.51).

Practice Problem A: Patterson and Hennessy problem 6.4

Practice Problem B: Patterson and Hennessy problem 6.5

Practice Problem C: Patterson and Hennessy problem 6.11: (Draw the pipeline timing diagram. When the clock strikes at the end of the 5th clock step, one general purpose register will get a new value and the `Read Data 1` and `Read Data 2` ID/EX pipeline registers will get new values read from two general purpose registers. Figure out which three of the general purpose registers these are.)

Problem 2: Patterson and Hennessy 6.23.

Problem 3: Patterson and Hennessy page 628, problems 7.7 and 7.8. (These are both problems about 16 word direct mapped caches.)

Problem 4: Patterson and Hennessy problem 7.32