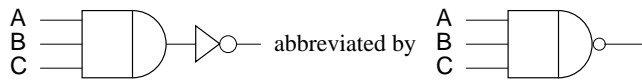


Readings: Patterson and Hennessy section B-5 (to page B-26), section B-4; Mano, sections 1-6 (concentrate on D flip-flops), 1-7, 2-4, 2-5 and 2-6.

Practice Problem A: Patterson and Hennessy (B.1), (B.2), (B.4), and (B.10). For B.10, after you write the four logic functions, verify each one on all 8 truth table rows.

Graded Problem 1:

- a. Mano page 37, problem 1-1. Proceed as in Patterson and Hennessy problem (B.6). Explain what it is about your truth table that “proves” the theorem.
- b. The three input NAND gate can be drawn as



Draw the circuit equivalent to it that has a three input OR gate and three inverters, and draw its abbreviation.

- c. The expression (14) $x + yx = (x + y)(x + z)$ claimed on page 8 of Mano to be an identity is a misprint. Find one combination of truth values for x , y and z that demonstrates this expression is not an identity.
- d. Correct expression (14) and use a truth table to prove that your correction is an identity. Hint: Try the distributive law of **OR** over **AND**. Identity (13) is the distributive law of **AND** over **OR**.

Graded Problem 2: Mano page 64 problem 2-11.

Graded Problem 3: Patterson and Hennessy second edition problem (B.21), plus:

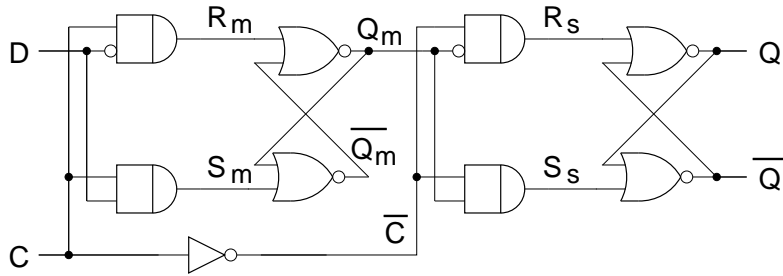
- a. Draw the finite state machine diagram as indicated and choose a clock speed that is appropriate for this application. When you write down the clock speed that you chose you must write the units in which it is measured. Hint: 1 Hertz (abbreviated Hz.) means 1 clock cycle per second. Units of clock speed (also called “frequency”) used to be called “cycles per second (CPS)” but in the 1960’s, the electrical engineering societies decided to honor Heinrich Hertz, an early explorer of radio waves, by using his name for these units.
- b. Assign the states of your finite state machine to combinations of bit values to be stored in flip-flops. Be sure it is clear how many flip-flops you are choosing to use. Assume that the state of each flip-flop will be **0** when the machine is turned on. Write in a table how the names of the states from your diagram correspond to combinations of flip-flop states.
- c. Write the state table for your design based on the state assignment you chose. It should have 3 output columns. The value for each output signal depends on the new state.
- d. The finite state machine will be implemented by D flip-flops. Write the logic equations for the D inputs and for the outputs. Draw the complete circuit diagram for your final design, using combinational gates and D flip-flops.

Graded Problem 4: Jump ahead and read section 5-4 of Mano. Implement the 4-bit sequence counter that would go in the box at the bottom of Figure 5-6 using D flip-flops. Show all work. Use either 4 variable Karnaugh maps or figure out the combinational logic using your knowledge of the binary numeral increment operation.

Graded Problem 5: First, complete the timing diagrams given out on Monday, Feb. 5 (do not hand in). Second, study the timing diagrams which express the behavior of the D flip-flop with falling edge trigger. In this problem you

will observe the details of how this behavior comes about when the D flip-flop is implemented with “master-slave” design.

Elaborate the D flip-flop implementation of Figure B.15 of Patterson and Hennessy by replacing the master and slave D transparent latches by their implementation given in Figure B.13. That means draw the circuit diagram on the next page: (“Elaboration” is a term about processing hardware designs given in a hardware description language such as VHDL that means replacing all higher level blocks with their definitions until the circuit is expressed only in terms of basic circuit elements.)



Notice the labels added for all the wires (nodes). Fill in the timing diagram below for the internal signals that result from the example of operation given in figure B.16.

