

Readings: Finish Appendix B of Patterson and Hennessy. Begin reading Patterson and Hennessy's section 4.5 and Mano's chapters 4 and 5. Refer back to earlier sections of Patterson and Hennessy's chapter 4 as needed to understand the meaning and implementations of arithmetic and logic operations. Observe how the material on combinational and sequential systems is applied in this description of a simple computer.

Graded Problem 1: Implement a 3 bit counter using D flip-flops that counts by 1s from 0 to 5, and then to 0, and repeats this sequence indefinitely. Thus it should have 6 states. Use the normal binary representation of the numbers for the combinations of flip-flop values. Write down the state diagram, state table, Karnaugh maps to determine minimal logic equations and the final circuit diagram. After writing down the final circuit diagram, write the calculations or provide screen image prints from software such as MMLogic that demonstrate you have verified your implementation.

What does your counter do if it is started in each of the two states that do not correspond to a count from 0 to 5? Think about what this problem suggests that practical computer hardware should do when it is first turned on.

Practice Problem A: Mano page 64 problem 2-3. Also, find out from your texts how and why decoders are used to build RAM (randomly accessible memory) systems.

Graded Problem 2: Mano page 64 problem 2-15: (a) Create an **interface specification** or outer view of the given 4-bit shift register. (b) Implement an 8-bit shift register with two of these given 4 bit shift registers. Part (b) is like the multiplexor problem from Homework 1.

Graded Problem 3: Patterson and Hennessy (B.7), to prove a Boolean algebra identity from axiomatic Boolean algebra identities.

Graded Problem 4: Patterson and Hennessy (B.9). Make up a non-trivial logic formula with 4 variables and demonstrate your algorithm on the formula you made up. Hint: Use the idea of the Binary Decision Diagram (BDD). The solution includes simplifying a logic formula after one of the variables is replaced by 1, and again by 0.

Graded Problem 5:

- The Boolean "implies" function $F(X, Y)$ denoted $X \Rightarrow Y$ is defined $X' + Y$. Write the truth table for this function. Then write an explanation of how it relates to mathematical statements of the form "If ... then"; your explanation must address the case when $X = 0$, that is, the "if" clause is FALSE. (Hint: Review CSI210 material on "implies".)
- Write the dual of the truth table for "implies": Interchange 0s and 1s everywhere, including the input column. Do not change the names of the variables.
- Write two Karnaugh maps, one for "implies" and the other for its dual.
- Write a simple boolean formula for the dual of "implies", based on the truth table you drew.
- Let F be a boolean formula, using the operators AND, OR and NOT, constants 0 and 1, and variables. The dual of F , denoted DF , is obtained by replacing AND by OR, OR by AND, 0 by 1, and 1 by 0 in F . Write the dual of $X' + Y$. Write the dual of $A'C' + B'C' + A'D' + B'D'$. Practice writing duals of other formulas.
- Compare:
 - The truth table of the dual of formula $F(X, Y) = X' + Y$.
 - The truth table you got above by "dualizing" the truth table of $X' + Y$.

Practice Problem B: Continue the timing diagram analysis of the SR latch, a problem from Homework 2: Suppose after both R and S have been at 1, they both go to 0 *simultaneously*. Explore what happens assuming (a) unrealistically both gates and wires have exactly equal delay times, and assuming (b) one gate is faster than the other.