The All-Minors VCCS Matrix Tree Theorem, Half-resistors and Applications in Symbolic Simulation

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ABSTRACT
The matrix tree theorem for directed graphs is generalized to cover all minors of nodal formulations of all linear circuits with voltage controlled current sources. The term signs are readily evaluated from linking-cycle-arborescence configurations in a common generalization of Maxwell’s and Coates’ rules. All minors are treated with the same formalism. The formulation introduces half-resistors which are transposed unistors. Their use for intuitive description of circuit operation based on approximation, nodal impedance conditions and backward error analysis is described for BJT amplifiers and the switch model for digital MOS circuits.

I. INTRODUCTION
Symbolic simulation of analog circuits has gathered recent attention with the development of improved algorithms, implementations and methods of application[1, 2]. The most important operation needed is to compute, symbolically, large minors (determinants of submatrices) of the indefinite admittance matrix:

$$
det A(S', V') = \sum_{F \in \mathcal{F}} \pm \prod_{e \in F} g_e = \sum_{F \in \mathcal{F}} \pm g_F
$$

where each $g_e$ is a symbolic complex or Laplace transform branch or mutual conductance parameter of circuit element $e$. Circuit node sets $S, V \subseteq N$ with $|S| = |V|$ are given; the corresponding rows and columns of $A$ are deleted to form the minor $det A(S', V')$, which is indexed by $S' = N - S$ and $V' = N - V$. While other more general system matrices have been used [3], the minors reduce to these when the all the elements are 2-terminal (resistor or complex impedance), 3-terminal or 4-terminal voltage controlled current sources. For large circuits, various kinds of circuit or matrix decomposition have been studied [4, 5]. The explicit cancellation free graph theoretic interpretation we give for every minor is therefore of interest.

Some current approaches use general determinant evaluation methods. This of course requires that cancellations among monomials that have been generated at different times be recognized and carried out, and a large number of cancelling monomials might be generated. For resistor-only networks, the set of uncanceled terms can be generated directly (with no cancellation) since each term corresponds to a spanning tree (or $k$-tree with specified roots when the minor is order $n - k$). The justification for this is from Maxwell’s rules and matrix tree theorems on undirected graphs. However, when general VCCSs are included two approaches have been developed to regain some of the advantages of these tree-sums.

The first approach[6, 7, 8] uses the separate graphs $U$ of the controlling (voltage) edges and $J$ of the controlled (current) edges, both of which are over the same circuit node set $N$. For each circuit element $e \in E$, there is exactly one edge in $U$ (denoted $U(e)$) and exactly one edge in $J$ (denoted $J(e)$). Each uncanceled term corresponds to a subset of elements $F \subseteq E$ whose image in $U$ is a forest and whose image in $J$ is also a forest. The forest in $U$ must be rooted at $V$; each tree must contain exactly one distinct node from $V$. Also, the forest in $J$ must be rooted at $S$. Each such $F$ can be called an $(S, V)$-complete forest which generalizes the term “complete tree” of Mayeda and Chen. The complete tree approach has been used with the tableau formulation [3] as well as the nodal formulation. In either formulation the sign determination is given in terms of several permutations including one for each of the two trees.

The second approach is based on the idea that each 4-terminal VCCS element can be simulated by 4 unistor elements [7, 8]. A unistor from $i$ to $j$ is a current source from $i$ to $j$ of value $gu_i$ where $u_i$ is the potential at node $i$. The four unistors have parameters $\pm g_e$. The resulting unistor network is naturally described by a single directed graph. The matrix tree theorem for directed graphs [7, 8, 9] can then be used to evaluate the minors. First, generating the rooted branchings is simpler than generating complete forests in $(J, U)$. The second advantage is that the sign of each term can be determined directly from the structure of the branching. The disadvantage is that the method is not cancellation-free.

In this paper we show how the cancellation free complete forest approach can be combined with the term sign determination of the directed $k$-tree approach. We express the sign using a combination of Maxwell’s and Coates
rules. These rules act on a directed graph of matrix $A$ that is a modification of the Coates graph. The modification distinguishes each arc $ij$, $i \neq j$ of weight $g_{e}$ that points into a node $j$ with a self-loop $jj$ of opposite weight $-g_{e}$ from arcs that do not. The self-loops are then omitted. The distinguished arcs are called half-resistor arcs. Half-resistor arc $ij$ contributes two entries to row $j$ of $A$; unistor arc $ij$ contributes to column $i$. The half-resistor from $i$ to $j$ sources current $g_{e}(u_{i} - u_{j})$ into node $j$.

An ordinary resistor can be represented by a pair of oppositely directed half-resistors. A 3-terminal VCCS corresponds to one half-resistor and two non-half-resistor arcs. These three arcs and corresponding entries in $A$ are shown below. The arc $bc$ is labelled active.

\[
\begin{array}{ccc}
 b & c & e \\
 e & \begin{array}{cc}
 -g_{e} & +g_{e} \\
 +g_{e} & -g_{e}
\end{array}
& A \\
\end{array}
\]

A 4-terminal VCCS has 4 non-half-resistor arcs. The half-resistor gives us strengthened necessary conditions that a set of elements corresponds to an uncancelled $\pm g_{e}$. When only half-resistors are present, the conditions become sufficient and our result reduces to the directed graph matrix tree theorem. The role of half-resistor $ij$ can be interpreted in two ways:

1. It is a VCCS with controlling port $ij$ that sources current from a reference node into node $j$.
2. When $ij$ is an ordinary resistor and we omit half-resistor $ji$, the resulting circuit represents an approximation made with the assumption that the current carried by the resistor from node $i$ is insignificant.

The latter interpretation is useful when we can know (with normalized voltages) that the nodal resistance of $j$ is much smaller than $g_{e}^{-1}$. This is discussed further in section V.

II. Matrix Tree Theorem

We are given $N = \{1, 2, \ldots, n\}$ and for each $v \in E$, distinct variable $g_{e}$. $A$ is formed from $n$ necessarily symmetric $A_{e}$ matrices with pattern of non-zero entries:

\[
A_{e} = \begin{bmatrix}
-g_{e} & -g_{e} \\
-g_{e} & -g_{e}
\end{bmatrix}
\quad \text{or} \quad
A = \sum_{e \in E} A_{e}.
\]

$D_{0}$ is the Coates graph of $A$. $D$ is the modification of $D_{0}$ in which each self-loop $jj$ is removed and $ij$ is distinguished as a half-resistor arc. Arc $ij \in D$ (note $i \neq j$) with label $e$ is active when $(A_{e})_{j,i} = +g_{e}$. The resulting directed graph contains the same flow information as the Coates or Mason’s graph.

Theorem 1

\[
\det A(S', V') = \epsilon(S)\epsilon(V) \sum_{F} \epsilon(\pi^{*})(-1)^{c_{y}(L)}(-1)^{\text{act}(L)}g_{F}
\]

where the sum is cancellation free and is over all $(S, V)$-complete forests relative to $J, U$. For each such $F$, there is a unique $L \subseteq D$ such that:

1. $L$ contains $|S| = |V|$ pairwise disjoint paths which define a matching $\pi^{*}: S \rightarrow V$ from the one path for each $s \in S$ that begins at $s$ and ends at $\pi^{*}(s)$.
2. $L$ contains $c_{y}(L)$ pairwise disjoint cycles that cover a subset of vertices that is disjoint from the vertices in the paths (1).
3. $L$ contains zero or more pairwise disjoint outwardly directed trees (branching of arborescences) rooted at the vertices in the linking paths (1) and the cycles (2). The non-root arborescence vertices comprise exactly the remaining vertices.

$\text{act}(L)$ is the number of active arcs in $L$. The $\epsilon$s are signs defined in III. Furthermore, (a) Each cycle of $L$ has at least one non-half-resistor arc and (b) The branching contains only half-resistor arcs.

When only half-resistor arcs are present as in the case of resistor only circuits, uncancelled cycles do not occur and the result reduces to the all minors directed graph matrix tree theorem[10]. Unfortunately, when non-half-resistor arcs are present, the the linking-cycle-arborescence constraints alone do not restrict us to uncancelled terms. However, once an uncancelled term is generated from an $(S, V)$-complete forest in $(J, U)$, our result will determine its sign.

The underlying mathematical phenomenon was described by Chen[6]. Terms that contain factors that derive from a set of self-loops in the Coates graph that correspond to a cycle will cancel with terms where those factors derive from that cycle in the Coates graph.

III. Sign Calculation

A matching $\pi : v' \rightarrow s'$ is a one-to-one correspondence from $v'$ onto $s'$. $(i, j)$ is an inversion when $i < j$ and $\pi(i) > \pi(j)$. Sign $\epsilon(\pi) = \exp(-1, \# \text{ inversions})$. Note

\[
\det A(S', V') = \sum_{\pi : S' \rightarrow v'} \epsilon(\pi) \prod_{i \in S'} A(\pi(i), i).
\]

Consider $\pi$ as a directed graph on $N$. Each vertex $v$ has indegree and outdegree 0 or 1, depending on whether $v \in S$ and $v \in V$ respectively. A part of $\pi$ decomposes into $|S| = |V|$ pairwise disjoint directed paths; each $s \in S$ is the first vertex of a path that begins at some vertex $\pi^{*}(s)$. If $s \in S \cap V$ then $\pi^{*}(s) = s$ and the path has one vertex and no arcs. The rest of $\pi$ decomposes into pairwise disjoint cycles. The vertices in cycles or interior to paths are $S' \cap V' = N - (S \cup V)$. It is shown in[10]:

\[
\epsilon(\pi) = \epsilon(\pi^{*})\epsilon(S)\epsilon(V) \times
\prod_{k} (-1)^{k} \prod_{m} (-1)^{m-1}
\]

Here, $\epsilon(T) = \exp(-1, \sum T)$. Substituting this formula into (1) generalizes Coates rule.
Theorem’s proof uses the factorization $A = I_J G^P_J$ ($I_J$ is the signed vertex-edge incidence matrix of graph $J$ and $G = \text{diag}(g_e, g_{e_2}, \ldots)$), the Cauchy-Binet theorem

$$\det A(S', V') = \sum_{F \subseteq E} I_J(S', F) \det I_{Jd}(V', F) g_F$$

and the fact that if $I_J(S', F)$ and $I_{Jd}(V', F)$ are both non-singular, then there are unique matchings $\pi_J : F \rightarrow S'$ and $\pi_{Jd} : F \rightarrow V'$ such that

$I_J(\pi_J(e), e) \neq 0$ and $I_{Jd}(\pi_{Jd}(e), e) \neq 0$ for every $e \in F$.

It follows that the $\pi$ in (1) that contributes to $\pm g_F$ is unique. The sign can therefore be determined either from $\epsilon(\pi) = \epsilon(\pi_J)\epsilon(\pi_{Jd})$ and the signs in the $A_{Jd}$'s, or from the signed linking-cycle decomposition of $\pi$ and count of active arcs. If the linking-cycle-foreborence $L$ has been constructed, $\pi^*$ can be computed in $O(n)$ time by depth-first search. However, if $\pi_{Jd}$ and $\pi_J$ are already available from $(S, V)$-complete forest generation, it might be more efficient compute their signs.

In either case it is useful to know that once a permutation or matching is available so that $\pi(e)$ can be obtained in constant time (for example, it is stored in an array), $\epsilon(\pi)$ and $\pi^*$ can be computed in linear ($O(n)$) time using array subscript operations. The sign of a matching $\pi : V' \rightarrow S'$ can be computed by counting the cycles in the permutation obtained by adjoining to $\pi$ arcs from the $k$th element of $V'$ to the $k$th element of $S$. Finding these arcs and computing $\epsilon(S)\epsilon(V)$ can be done in linear time by a forward scan of arrays of length $n$.

IV. Example

![Diagram](https://via.placeholder.com/150)

<table>
<thead>
<tr>
<th>b</th>
<th>$G_B + g$</th>
<th>$G_E$</th>
<th>$G_C$</th>
</tr>
</thead>
<tbody>
<tr>
<td>c</td>
<td>$g_m + g_e + g_{ee}$</td>
<td>$-g_{ee}$</td>
<td>$-G_{ee}$</td>
</tr>
</tbody>
</table>

V. Approximate Circuits

Every individual occurrence of an element parameter $g_e$ in the matrix $A$ might be identified with a physical effect that contributes to the operation of the circuit. Often the identification of effects and their contribution is easier when several occurrences of $g_e$ are considered together. Consider a resistor $e$ between nodes $i$ and $j$. The two occurrences $g_e$ in $A_{ij}$ and $-g_e$ in $A_{ji}$ represent the effect that the resistor conducts current of magnitude $g_e(u_i - u_j)$ to flow into node $j$. The other two occurrences of $\pm g_e$ in $A_{ii}$ and $A_{jj}$ represent the effect that the current flows from the other node $i$. Now if the nodal resistance of node $j$ is very small compared to $g_e^{-1}$ but the nodal resistance of $i$ is comparable to $g_e^{-1}$, the first effect on determining $u_j$ might be insignificant while the second will be very significant in determining $u_i$. To model this heuristic observation, let us write

$$A = A^\text{App} + A^\text{Err}$$

where $A^\text{Err}$ is formed from the occurrences of parameters in $A$ that we want to verify are insignificant. The node equations are

$$A(N^\text{Var}, N^\text{Var})u + A(N^\text{Var}, N^\text{Con})U^\text{Con} = I$$

where $N^\text{Con}$ is the set of nodes tied to external potential sources with values $U^\text{Con}$. $J$ is the vector of values of external current sources tied to nodes $N^\text{Var} = N - N^\text{Con}$, and $u$ is the solution of node potentials on $N^\text{Var}$. Let $u^\text{App}$ solve the approximating system

$$A^\text{App}(N^\text{Var}, N^\text{Var})u^\text{App} + A^\text{App}(N^\text{Var}, N^\text{Con})U^\text{Con} = I$$

The approximation errors $u^\text{err} = u^\text{App} - u$ are shown to be the solution to the system

$$A^\text{App}(N^\text{Var}, N^\text{Var})u^\text{err} = A^\text{Err}(N^\text{Var}, N^\text{Var})u +$$

The right hand side represents currents in the original circuit that are assumed to have insignificant effect. For normalized voltages, these currents are bounded above by the arc conductances. The inverse of $A^\text{App}(N^\text{Var}, N^\text{Var})$ is the matrix of nodal resistances in the approximating circuit. Thus, errors that occur in modeling the original circuit represented by $A$ by an approximating circuit with matrix $A^\text{App}$ are referred back as additional inputs to the approximating circuit. The usefulness of (2) is that the approximation errors can be understood by analyzing the effects of the additional inputs to the approximating circuit rather than as perturbations to the original circuit. This backward error analysis idea is used to analyze the effect of round-off errors in numerical computation[11]—here we apply it to analyze modeling errors.
A. Basic BJT Amplifiers

To illustrate, we analyze the input section of a CE emitter degenerated BJT amplifier under the hypothesis that \( g_m \gg G_E \) and \( r_e \) is insignificant. The approximating circuit below is for \( u_b \) and \( u_e \).

\[
\begin{align*}
\overline{U_B} & \quad \overline{G_B} & \quad \overline{U_E} \\
\overline{b} & \quad \overline{g_m} & \quad \overline{e} \\
\overline{r_n} & \quad \overline{G_E} \\
\end{align*}
\]

\[
\begin{align*}
\frac{u_b}{u_e} &= \frac{g_m}{G_E} \\
\frac{u_e}{-G_B} &= \frac{u_e}{-G_B} \\
\end{align*}
\]

The solution is \( u_b = u_e = U_B \). The node resistances in this approximating circuit are \( R_{bb} = G_E^{-1} \) and \( R_{ce} = g_m^{-1} \).

Since the elements are passive, theorem 1 can be used in general to show the transfer resistances \( R_{bc} \leq R_{ce} \) and \( R_{eb} \leq R_{bb} \). In this simple circuit we have in fact \( R_{bc} = 0 \) and \( R_{eb} = R_{bb} \). To check the validity of the approximation, assume \( U_B - U_E = 1 \) and observe that the true emitter current \( (G_E) \) is no more than \( G_E \). The true current in \( r_n \) is no more than \((h_{fe} + 1)^{-1}G_E \). Therefore the error in taking \( u_b = U_B \) is no more than

\[
R_{bb}(h_{fe} + 1)^{-1}G_E + R_{bc}G_E = G_E^{-1}(h_{fe} + 1)^{-1}G_E.
\]

Similarly the error in taking \( u_e = U_B \) is no more than

\[
R_{ce}G_E + R_{eb}(h_{fe} + 1)^{-1}G_E = [g_m^{-1} + G_E^{-1}(h_{fe} + 1)^{-1}]G_E
\]

Consider another case where \( R_B \) is very large—the amplifier is driven by an approximate current source \( G_B \cdot 1 \). The relevant approximating circuit is now

\[
\begin{align*}
\overline{U_B} & \quad \overline{G_B} & \quad \overline{U_E} \\
\overline{b} & \quad \overline{g_m} & \quad \overline{e} \\
\overline{r_n} & \quad \overline{G_E} \\
\end{align*}
\]

with solution \( u_b = u_e = U_E \) and \( R_{bb} = g_m g_{\pi}^{-1} G_E^{-1} + G_E^{-1} + g_{\pi}^{-1} \) and \( R_{eb} = G_E^{-1} + g_m g_{\pi}^{-1} G_E^{-1} = (h_{fe} + 1)G_E^{-1} \). The error in \( u_b \) is no more than

\[
[(h_{fe} + 1)G_E^{-1} + g_{\pi}^{-1}]G_B
\]

and the error in \( u_e \) is no more than

\[
(h_{fe} + 1)G_E^{-1}G_B.
\]

B. Switch Model for Digital MOS

The switch model[12] enables rapid logical simulation implemented with graph theoretic path finding techniques. It encompasses the bidirectional, ratioed logic, charge sharing and charge storage design techniques of digital CMOS. Roughly, series and parallel connection of conductions are switch modelled by \( \text{min} \) and \( \text{max} \) respectively.

We have found[13] that half-resistors provide a linear circuit theoretic model for the switch model rules, which include: A closed switch \( ij \) with conductance (strength in [12]) \( g \) between node \( i \) of strength \( \gg g \) and node \( j \) of strength \( \approx g \) will propagate the signal value at \( i \) to affect \( j \) but not vice-versa. In general we can construct a linear circuit whose node voltages \( u \) are precisely \( 0 \) or \( 1 \) where the switch model predicts a definite \text{FALSE} or \text{TRUE}, and

\[0 < u < 1\] otherwise. With our linear model, the linear nodal conductance and error analysis as outlined above can be used to assess the validity of the switch modelling. The directed graph version of the matrix tree theorem is useful to relate linear circuit properties to those of the switch graph.

VI. Conclusion

Symbolic simulation of an approximating circuit might produce fewer terms than exact symbolic simulation. The validity of the results might be assessed by comparing the nodal resistances from the approximating circuit to parameter values of effects that the approximation ignores. This is an alternative to approximation methods ([5, 3] for example) based on omitting monomials from the final result of exact symbolic simulation based on estimates of those monomials’ numeric values.

References