

# CSI504–Computer Organization Spring 2000–Course Announcement

Instructor: Prof. Seth Chaiken, LI96H, 442-4282, sdc@cs.albany.edu (Office hours: TBA)

Class meeting: Tuesday and Thursdays, 8:15AM-9:35AM, Business Adm. Bldg.-213

This graduate course is a second course in computer architecture and organization. It is about the interface between computer hardware and software with the emphasis on hardware. This subject will help you to understand new developments in conventional computer hardware and how software can take advantage of them. How computer speed is reported and the kinds of quantitative analysis methods used by computer designers today to predict overall system performance will be covered. The course text is the second edition (1995) of *Computer Architecture A Quantitative Approach* by John L. Hennessy and David A. Patterson, Morgan Kaufmann, Inc. These authors are the researchers who helped to develop the RISC (reduced instruction set computer) concept to its position as the basis for high performance microprocessors for the 1990's. Supplemental readings from the Web or Library Reserve may be assigned on topics such as VHDL and performance modeling/measurement.

**Prerequisites:** Knowledge of one machine language, its assembler and one or more languages such as C++, C or PASCAL, combinational and sequential circuit design, and CPU and memory hardware implementation. The required background is equivalent to CSI404 or the acquaintance with the first eight chapters of *Computer Engineering Hardware Design* by M. Morris Mano. The text *Computer Architecture and Organization* by John P. Hayes is recommended as an advanced reference on the required background. Hennessy and Patterson have also published an undergraduate text *Computer Organization & Design the Hardware/Software Interface*, Morgan Kaufmann, 1994 which includes details of assembly language programming (for the MIPS instruction set architecture) and of computer hardware design.

CSI504 is a graduate elective course. In addition to the usual lectures and written homework assignments, there will be some computer experiments based on standard Unix and software provided with the text. Every student will also present a half-hour summary with critical remarks of a recent computer architecture research paper to a seminar to be conducted toward the end of the semester. Extra class meetings will be scheduled at that time. Briefly, the report will cover a paper in a recent ACM/IEEE Symposium on Computer Architecture or ASPLOS conference proceedings, ACM Trans. on Computer Systems, or similar refereed publication. The report must both relate the topic to specific lecture or textbook material, and summarize the reported results.

The homework problems will be collected and checked for general correctness, clarity and completeness, and graded on a scale of 0-4 per problem. Late homework will be accepted until the next class meeting with a penalty of 1 point per late problem. Since TA resources are not available, I cannot do much detailed correction. You will be responsible for material on solution handouts, which will be covered in examinations. Other resource limitations prevent me from awarding an I (incomplete) grade except if the course work is at least B level *as of* the drop day and a genuine, documented extenuating circumstance occurs *after* the drop day.

The syllabus items and associated topics follow.

1. Factors that affect computer cost and performance, and quantitative evaluation and comparison thereof. Speedup, balances and tradeoffs, historical trends, costs, benchmarks.
2. Review of instruction set architecture possibilities, their relationship to performance.
3. Implementation of pipelined processors. Parallelism, hazards, stalls and how they are avoided or controlled. Hardware and software approaches to improving performance.
4. Memory systems, caches. Principles of locality and memory hierarchy, virtual memory, protection, multiprocessing and concurrency issues, related machine instructions.
5. Input/output and system interconnection hardware. I/O devices, busses, interrupts and related instructions, coprocessors, performance evaluation.
6. Additional topics may include VHDL, arithmetic algorithms, networks and parallel processing.

Grading: Two in-class midterms: Thu., Feb. 24 and Thu., Apr. 6 (20% each), final May 18 10:30AM-12:30PM (30%), report (15%), homework (15%).